REMARKS/ARGUMENTS

This paper is responsive to the Office Action dated December 10, 2003, having a shortened statutory period expiring on March 10, 2004, wherein:

Claims 1-85 were previously pending in the application; and

Claims 1-85 were rejected;

Claims 7 and 36 have been amended, no claims have been added, and claims 15 and 16 have been canceled without prejudice or disclaimer of the subject matter recited therein by this amendment. Accordingly, claims 1-14 and 17-85 remain currently pending in the present application.

Information Disclosure Statement(s)

In the present Office action, the Examiner indicated that Information Disclosure Statements submitted by Applicants on July 19, 2001 and November 10, 2003 failed to provide a legible copy of each U.S. and foreign patent and each publication or that portion which caused it to be listed as required by 37 CFR §1.98(a)(2). Applicants respectfully disagree in part. 37 CFR §1.98(d) provides that:

> A copy of any patent, publication, pending U.S. application or other information, as specified in paragraph (a) of this section, listed in an information disclosure statement is required to be provided, even if the patent, publication, pending U.S. application or other information was previously submitted to, or cited by, the Office in an earlier application, unless: (1) The earlier application is properly identified in the information disclosure statement and is relied on for an earlier effective filing date under 35 U.S.C. 120; and (2) The information disclosure statement submitted in the earlier application complies with paragraphs (a) through (c) of this section.

Applicants respectfully submit that, with the exception of the U.S. Patent Applications listed under the "Other Art" section of the Information Disclosure Statement submitted by Applicants on November 10, 2003, all references indicated in the above-identified Information Disclosure Statements comply with 37 C.F.R. §1.98(d). Consequently, Applicants request that the remaining references be considered and that the Examiner indicate his consideration of these references using the previously supplied PTO Form-1449.

Rejection of Claims under 35 U.S.C. § 102

In the present Office Action, claims 1-85 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,357,249 issued to Azaren, et al. (hereinafter, "***Azaren***"). While not conceding that the Examiner's cited reference(s) qualify as prior art, but instead to expedite prosecution, Applicants have chosen to respectfully disagree and traverse the rejection as follows. Applicants reserve the right, for example, in a continuing application, to establish that one or more of the Examiner's cited references do not qualify as prior art as to an invention embodiment previously, currently, or subsequently claimed. With regard to Applicants' claims 1, 18, 24, 30, 56, and 66, the Examiner states within the present Office Action that ***Azaren*** discloses a method of communicating a data stream through a telecommunications system comprising:

> Rearranging said data stream into a serial optical signals (second plurality of words), wherein said second plurality of words include a synchronization bit pattern (relock word), and...col. 6, lines 40-55...
>
> for each of said second plurality of words, determining if said each of said second plurality of words should be included in the generation of a backplane parity value by determining if said each of said second plurality of words is synchronizing or not (relock word). Col. 5 lines 45-46.

Applicants respectfully disagree and submit that ***Azaren*** fails to teach "determining if said each of said second plurality of words should be included in the generation of a backplane parity value by determining if said each of said second plurality of words is said relock word" (emphasis supplied) as required by Applicants' claim 1, and generally required by Applicants' claims 7, 18, 24, 30, 36, 46, 56, 66, and 76. At Column 6, Lines 40-55 and Column 5, Lines 45-46, ***Azaren*** teaches an ID/Synch Logic Circuit 68 used to produce "an alternating '0' and '1' synchronization pattern" and to allow parity bits to be inserted into frames of a digital data signal as well as that, "...bit errors are not counted until frame synchronization is acquired."

The Examiner's cited portion of ***Azaren*** fails to teach however, a determination if each of the described "serial optical signals" is either a synchronization bit pattern or "synchronizing" and consequently cannot be construed as teaching, "determining if said each of said second plurality of words is said relock word" as claimed. ***Azaren*** teaches the insertion of an alternating "0" and "1" synchronization pattern into the first

"synchronization" frame bit of every fourth frame transmitted (see ***Azaren***, Column 5, Lines 25-29) as well as additional parity and channel identification frame bits (***Azaren***, Abstract, see also ***Azaren***, Figure 3). ***Azaren*** further teaches a frame detection circuit which, "accepts the frame bit...and determines the synchronization frame bits of the input data..." (***Azaren***, Column 10, Lines 13-16). The operation of frame detection circuit 106 is more fully described at column 11 which teaches in relevant part,

> Frame detector logic circuit 106 receives as an input the frame bit from register 134 of serial-to-parallel logic circuit 102 as discussed above. This frame bit is input into a series of four slave state latches...[and] transferred from the left farthest state latch to the next consecutive three latches at the sample clock frequency. Each of the outputs I1-I4 of the latches are applied to an acquisition state machine circuit 146 having four individual acquisition state machines (not shown). The acquisition state machine circuit 146 is configured to look for the 32-bit alternating 0-1 sequence of sync frame bits in order to determine sync acquisition. Since the sync bit is only one bit of the four frame bits, the acquisition state machines are loaded at a rate of the sample clock divided by four as shown. (***Azaren***, Column 11, Lines 5-23)

Applicants therefore respectfully submit that ***Azaren*** fails not only to teach a determination of whether each "parallel digital data signal" or "serial data signal" is either a synchronization bit pattern or "synchronizing" but further whether even each frame bit is a synchronization bit pattern or "synchronizing". Consequently, Applicants respectfully submit that ***Azaren*** fails to teach, "determining if <u>said each of said second plurality of words</u> is said relock word" as claimed (emphasis supplied). For at least the foregoing reasons, Applicants submit that Applicants' claim 1, as presented, is allowable over ***Azaren*** and request that the Examiner's current rejection(s) be withdrawn. Applicants' claims 7, 18, 24, 30, 36, 46, 56, 66, and 76 each contain one or more limitations substantially similar to those described with respect to Applicants' claim 1 and are therefore allowable for at least those reasons stated for the allowability of claim 1. All remaining claims, depending directly or indirectly from Applicants' claims 1, 7, 18, 24, 30, 36, 46, 56, 66, and 76 are similarly allowable over ***Azaren*** for at least the reasons stated herein.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5097.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Non-Fee Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on 3/5, 2004.

Attorney for Applicant(s) — Date of Signature: 3/5/04

Respectfully submitted,

Justin M. Dillon
Attorney for Applicants
Reg. No. 42,486
(512) 439-5097 [Phone]
(512) 439-5099 [Fax]